ABSTRACT

A digital signal processor having priority logic coupled to an array of storage elements, the priority logic to provide to a priority signal lines an indication of a location of a particular number in the array of storage elements. The priority logic includes compare circuits where each compare circuit is coupled to one of the storage elements in the array of storage elements. Each compare circuit has a first input coupled to a storage element, a second input coupled to a match line, and an input/output line coupled to one of the priority signal lines. The priority logic also includes a delay circuit coupled to each of the compare circuits.